UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/699,827	11/04/2003	Kazuhisa Sakihama	244844US2S	5577

22850 7590 09/22/2004

OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
KITOV, ZEEV	

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 09/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/699,827	SAKIHAMA ET AL.	
	Examiner	Art Unit	
	Zeev Kitov	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/04/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The Specification is objected to due to a following reason. The Fig. 12 circuit description given on pages 27 and 28 includes some contradictory statements. For example transistor N2 turning on forces the thyristor to turn off (Page 27, lines 18 –19), while the same transistor turning on another time forces the thyristor to turn on. Supposedly, the difference should be in a presence or absence of ESD event. However, it is not clearly stated.

According to the best understanding of the Examiner, when N-MOS transistor turns on, it should automatically lead to a saturation of the NPN transistor 95 and activation of the thyristor; no ESD event is necessary for that.

Additionally, it is not clear how turning on of the transistor N1 can force transistor N2 into conductive state. The N2 is the NMOS transistor and to turn it on one has to apply to the transistor's gate the potential higher than the substrate potential. No matter whether the substrate is connected to the source (the upper terminal of the transistor according to the Specification) or to the drain (the bottom terminal of the transistor), there is no potential high enough to drive it into on state when N1 is on. Appearance of the voltage across the resistor R can result only in turning N2 off. As a result, the thyristor cannot be fired.

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, "the fourth MOS transistor of a second conductivity type, whose source is connected to the first pad and whose gate is connected to the output terminal of the inverter circuit, and a first resistor element which is connected at one end to a drain of the fourth transistor and at the other end to the second pad" of Claim 10 should be shown according to the claim language or the feature(s) canceled from the claim(s). No new matter should be entered. As a matter of fact, neither Fig. 11, nor Fig. 12 shows all the elements of the claim. No new matter should be entered.

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the first and second pads of Claim 8 should be shown according to the claim language (emitter connected to the first pad) or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for

consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

1. Claim 10 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 10 is dependent on Claim 8, which discloses the PNP bipolar transistor having its base connected to the output of the inverter. Further, according to the claim 10, the fourth MOS transistor having a resistor in series with its drain and a gate being connected to the output of the inverter. So there is no connection between the fourth MOS transistor and the PNP transistor when they both are controlled by the output of the inverter. Such structure is neither disclosed in

the Specification, nor illustrated in Drawings. The purpose of such circuit and its way of action are unclear.

2. Claim 11 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 11 is dependent on Claim 9, which discloses the thyristor element. Claim 11 adds the limitation of the fourth MOS transistor of a second conductivity type; the circuit is illustrated in Fig. 12. However, it is not clear how turning on of the transistor N1 can force transistor N2 into conductive state. The N2 is the NMOS transistor and to turn it on one has to apply to the transistor's gate the potential higher than the substrate potential. No matter whether the substrate is connected to the source (the upper terminal of the transistor according to the Specification) or to the drain (the bottom terminal of the transistor), there is no potential high enough to drive it into on state when N1 is on. Appearance of the voltage across the resistor R can result only in turning N2 off. As a result, the thyristor cannot be fired.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

1. Claim 16 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant

regards as the invention. A reason for that is a following phrase: "programmed in accordance with whether a semiconductor chip including the semiconductor integrated circuit has been incorporated into an end product". It is not clear how the fact of incorporation into an end product can affect a way of programming of the control circuit. For purpose of examination it was interpreted as follows: "programmed after a semiconductor chip including the semiconductor circuit has been incorporated into an end product".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by Ker et al. (US 6,249,410), further called Ker 1. Ker 1 discloses all the elements of Claim 1 including an ESD protection circuit including: a first pad (element 300 in Fig. 12) used as an external connection terminal to be connected to a semiconductor integrated circuit; a second pad (element 305 inFig.12) used as an external connection terminal to be connected to the semiconductor integrated circuit; a clamp circuit (element 310 in Fig.12) connected between the first pad and the second pad; and a control circuit (element 345 in Fig.12) controlling the clamp circuit, rendering the same conducting or non-conducting.

Regarding Claim 2, Ker 1 discloses the clamp circuit as a switch element rendered to be conducting or non-conducting in accordance with a control signal output from the control circuit (col. 11, line 61-col. 12, line 19).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3 - 6 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ker 1 in view of Ker et al. (US 5,959,820), further called Ker 2. As was stated above, Ker 1 discloses all the elements of Claim 1. However, regarding Claim 3, it does not disclose an inverter. Ker 2 discloses the inverter circuit (NMOS and PMOS transistors inside block 204a in Fig. 13a) receiving a control signal from the control circuit (element 204a in Fig. 13a), and a switch circuit (element 202 in Fig. 13a) which is turned on or off by an output signal of the inverter circuit. Both references have the same problem solving area, namely providing ESD protection for the semiconductor circuits. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Ker 1 solution by adding the inverter according to Ker 2, because as Ker 2 states (col. 8, lines 33 – 47), the inverter is

necessary for inverting the signal, i.e. for sending the signal to the switching element with an appropriate logic level.

Regarding Claim 4, Ker 2 discloses the inverter circuit comprises a first MOS transistor of a first conductivity type (the top transistor in the block 204a in Fig. 13a), whose source is connected to the first pad and whose gate is connected to receive the control signal from the control circuit, and a second MOS transistor of a second conductivity type (the bottom transistor in the block 204a in Fig. 13a), whose drain is connected drain of the first MOS transistor, whose source connected to the second pad, and whose gate is connected to receive the control signal from the control circuit. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Ker 1 solution by adding transistors of different polarity according to Ker 2, because this is well known in the art solution to control both upper and bottom transistors by a single signal.

Regarding Claims 5 and 6, Ker 1 discloses the switch circuit having a third MOS transistor (element 310 in Fig.12) of the second conductivity type (N-type MOS), whose drain is connected to the first pad (element 300 in Fig.12), whose source is connected the connected to an second pad (element 305 in Fig. 12); In the Ker 1 circuit modified according to Ker 2, the gate of the transistor is connected to an output terminal of the inverter circuit.

Regarding Claim 9, Ker 2 discloses the switch circuit including a thyristor (elements NCLSCR1 – NCLSCRn in Fig. 10a) whose anode and cathode are connected between the first pad and the second pad, and a trigger circuit (element 204

in Fig. 10a), which supplies a trigger current to the thyristor to turn on or off the thyristor. Both references have the same problem solving area, namely providing ESD protection for the semiconductor circuits. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Ker 1 solution by replacing the MOS transistor by the thyristor according to Ker 2, because as Ker 2 states (col. 1, lines 49 – 55), it has a great bypassing current, which is especially essential for the ESD protecting circuit with limited area.

Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ker 1 in view of Ker 2 and Bishop et al. (US 5,272,371). As was stated above, Ker 1 and Ker 2 discloses all the elements of Claims 1 and 3. However, regarding Claim 7, they do not disclose the switch circuit comprises an NPN bipolar transistor. Bishop et al. disclose an NPN bipolar transistor (element 113 in Fig. 5b) whose collector is connected to the first pad and emitter is connected to the second pad. In the Ker 1 circuit modified according to Ker 2, the base of the transistor is connected to an output terminal of the inverter circuit. Both references have the same problem solving area, namely providing ESD protection for the semiconductor circuits. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Ker 1 solution by replacing the MOS switch by the NPN NPN bipolar transistor according to Bishop et al., because as Bishop et al. state (col. 3, lines 12 – 14) the bipolar transistors conduction is an effective method of safely conducting charge during an ESD event and additionally, as well known in the art, the parasitic bipolar

lateral transistors are readily available as complement to the regular MOS structure; therefore their manufacturing is an easy technological process.

Regarding Claim 8, Bishop et al. disclose the PNP transistor (element 13 in Fig. 1). The motivation for modification of the primary reference is the same as above.

Claims 12 - 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ker 1 in view of Ker 2 and Metz et al. (US 5,400,202). As was stated above, Ker 1 and Ker 2 discloses all the elements of Claims 1 and 3. However, regarding Claim 12, they do not disclose the control circuit rendering the clamp circuit conducting when no power is supplied to the semiconductor integrated circuit, and rendering the clamp circuit non-conducting when power is supplied to the semiconductor integrated circuit. Metz et al. disclose the control circuit (elements 42, 40 18 in Fig. 4a, col. 6, line 42 – col. 7, line 9) rendering the clamp circuit conducting when no power is supplied to the semiconductor integrated circuit, and rendering the clamp circuit non-conducting when power is supplied to the semiconductor integrated circuit. Both references have the same problem solving area, namely providing ESD protection for the semiconductor circuits. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Ker 1 solution by adding the control circuit with features according to Metz et al., because as well known in the art, an integrated circuit can be damaged by an electrostatic discharge from the technician fingers while touching the unpowered integrated circuit.

Regarding Claim 13, Metz et al. disclose a third pad (the leftmost Vdd pad in Fig. 4a) connected to the control circuit; in the Ker 1 circuit modified according to Metz et al. the control circuit will render the clamp circuit active, or conducting, when no potential is applied to the third pad, and will render the clamp circuit non-active, or non-conducting, when a predetermined potential (Vdd) is applied to the third pad.

Regarding Claim 14, Metz et al. disclose a resistor R connected between the gate of the NMOS transistor and to a ground potential to maintain the potential on the gate of the NMOS trigger FET (col. 6, lines 49 – 50). By analogy, similar resistor can be connected between the third pad and a first potential source, i.e. between the gate of transistor 42 in Fig. 4a of Metz et al. and the ground terminal. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Ker 1 solution by adding the load circuit (resistor) to the third pad according to Metz et al., because according to Metz et al. (col. 6, lines 49 – 50), such load (resistor) is necessary to maintain the potential on the gate of the NMOS FET; such load resistor will prevent the MOS transistor connected to the third pad from inadvertent turning on.

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ker 1 in view of Ker 2 and Metz et al. and further in view of Court Decision *St. Regis Paper Co. v. Bemis Co.,* 193 USPQ 8. As was stated above, Ker 1, Ker 2 and Metz et al. disclose all the elements of Claims 1, 13 and 14. However, regarding Claim 15, they do not disclose a second resistor. The Court Decision addresses this issue by stating that

mere duplication of the essential working parts of a device involves only routine skill in the art. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Ker 1 solution by adding the second resistor, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art.

Claims 16 and 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ker 1 in view of Lee et al. (US 6,365,938). As was stated above, Ker 1 and Yu disclose all the elements of Claim 1. However, regarding Claims 16 and 17, they do not disclose the programmable circuit having a fuse element. Lee et al. disclose the programmable circuit having the fuse element (elements h in Fig. 5 and 7, col. 6, lines 14 - 28) that is cut after the semiconductor chip is incorporated into the end product, and the semiconductor chip has fourth and fifth pads (end points 7 and 7' on the line 126a in Fig. 5), which supply a current to the fuse element to cut the fuse element after the semiconductor chip incorporated into the end product. Both references have the same problem solving area, namely protecting the semiconductor circuits against electrical damage including the plasma processing. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Ker 1 solution by adding the fuse structure according to Lee et al., because as Lee et al. state (col. 1, lines 39 – 48), such structure is necessary for the plasma processing step only and for normal functioning afterwards should be removed.

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ker 1 in view of Lee et al. and Nguen (US 5,682,049). As was stated above, Ker 1 and Lee et al. disclose all the elements of Claims 1 and 16. However, regarding Claim 18, they do not disclose third and fourth resistors. Nguen discloses the fuse circuit (elements 66 and 65 in Fig. 4) including the third resistor (elements R3 and R0 in Fig. 4) connected between the fuse element and a first potential source, i.e. emitter of transistor (element 61 in Fig. 4) and the fourth resistor (element R2 in Fig. 4) connected between the other end of the fuse element and a second potential, i.e. ground potential. Both references have the same problem solving area, namely adjusting the resistance and voltage values by using fuses. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Ker 1 solution by adding the third and the fourth resistor according to Nguen, because trimming an electrical value potential according to Nguen would adjust the threshold value of the Ker 1 system modified according to Lee et al. to a proper functioning level. Such adjustment of the threshold is necessary to meet demands of different customers, which have different values of the supply voltage and therefore need different threshold values of protection mechanism.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zeev Kitov whose current telephone number is (571) 272 - 2052. The examiner can normally be reached on 8:00 – 4:30. If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571) 272 – 2800, Ext. 36. The fax phone number for organization where this application or proceedings is assigned is (703) 872-9306 for all communications.

Z.K.
09/13/2004